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SPECIFICATION

1. TITLE OF INVENTION

Hybrid Integrated Circuit Device

2. CLAIMS

(1) A hybrid integrated circuit device, comprising a circuit board with a through hole having a specified shape formed in a desired portion thereof, a wire conductor provided at the first surface of this circuit board and extending from the edge of said through hole, a semiconductor chip having an electrode formed in a region in the center of one main surface that is the same shape as the shape of said through hole and the peripheral part of said main surface is secured to the second surface of said circuit board so that said electrode formation region coincides with said through hole, and a bonding wire passing through said through hole to connect said semiconductor chip electrode and said wire conductor.

(2) The hybrid integrated circuit device recited in claim 1, wherein an insulator is provided at the second surface of the circuit board; the insulator has a thickness greater than the thickness of the semiconductor chip, and a through hole with a shape larger than the external dimensions of said semiconductor chip is formed therein at a part corresponding to the securing location of said semiconductor chip on said second surface.

3. DETAILED DESCRIPTION OF THE INVENTION

The present invention pertains to a hybrid integrated circuit device (hereinafter "HIC") that mounts a semiconductor chip and external components on a circuit board.

FIG. 1(A) is a plan view showing the mounting part of a semiconductor chip on a circuit board in one example of a conventional HIC. FIG. 1(B) is a sectional view along line IB-IB in FIG. 1(A).

In the drawings, (1) is a circuit board with an indentation (1a) provided at one part of its surface, (2) is a plurality of wire conductors formed at the upper surface of the circuit board (1) so as to extend from the upper end of the side walls of the indentation (1a), (3) is a semiconductor chip with a plurality of electrodes (not shown in drawing) formed at specified intervals alternatingly along the edges of its first main surface and with its second main surface secured to the bottom of the indentation (1a), (4) is a bonding wire connecting the semiconductor chip (3)'s electrode (not shown in drawing) with the corresponding wire conductor (2), and (5) is a chip coat consisting of a resin such as silicone, epoxy, etc. and spreading from inside the indentation (1a) across part of the surrounding surface of the circuit board (1) and covering specified parts of the semiconductor chip (3), bonding wire (4), and wire conductor (2) and protecting the semiconductor chip (3) from external air.

Incidentally, this conventional HIC is the so-called wire bonding type, in which the second main surface of the semiconductor chip (3) is soldered to the bottom of the circuit board (1)'s indentation (1a) and each of the semiconductor chip (3)'s electrodes is connected to the wire conductor (2) corresponding to those electrodes by a bonding wire (4); so the mounting area of the semiconductor chip (3) on the circuit board (1) is larger than the area of the main surface of the semiconductor chip (3). Therefore it has the problem of being disadvantageous when the circuit board (1) requires miniaturization, as when an HIC is used in a watch or the like. In addition, the adhesion area between the chip coat (5) and the circuit board (1) is also large, so much stress is created inside the chip coat (5) due to the difference between the coefficient of thermal expansion of the circuit board (1) and the coefficient of thermal expansion of the chip coat (5), and the bonding wire (4) may break because of this stress, leading to the problem of bad reliability. The conventional means of solving this sort of problem is the so-called flip chip system, in which the semiconductor chip (3)'s plurality of electrodes all become projecting electrodes, and these projecting electrodes are simultaneously soldered to the wire conductors (2) corresponding to them. However, in this flip chip system the mounting area of the semiconductor chip (3) with its projecting electrodes on the circuit board (1) becomes identical to the area of the main surface of the semiconductor chip (3), so it is possible to miniaturize the circuit board (1), but the price of a semiconductor chip (3) with projecting electrodes is vastly higher than the price of a semiconductor chip (3) without projecting electrodes used in the wire bonding system. Also, it is not easy to simultaneously solder each projecting electrode of a projecting-electrode-type semiconductor chip (3) to the corresponding wire conductor (2) in a satisfactory manner, so manufacturing yield in the flip chip system is worse than manufacturing yield in the wire bonding system, and the manufacturing cost is also higher. These are defects.

The present invention considered the defects described above, so its object is to provide an HIC that miniaturizes the shape of the circuit board and achieves a low price by improving the structure of a semiconductor chip and circuit board so as to reduce the semiconductor chip's mounting area on the circuit board while using the wire bonding system.

FIG. 2(A) is a plan view showing the mounting part of a semiconductor chip on a circuit board in an HIC that is one embodiment of the present invention. FIG. 2(B) is a sectional view along line IIB-IIB in FIG. 2(A).

In the drawings, (11) is a circuit board with a through hole (11a) having a specific shape formed in a desired part thereof, (12) is a plurality of wire conductors formed at the first surface of the circuit board (11) so as to extend from the edge of the through hole (11a), (13) is a semiconductor chip with a plurality of electrodes (not shown in drawing) formed within a region in the center of one main surface with the same shape as the shape of the through hole (11a); the peripheral part of the semiconductor chip (13) is bonded to the second surface of the circuit board (11) with adhesive so that the semiconductor chip (13)'s electrode formation region coincides with the through hole (11a). (14) is a bonding wire passing inside the through hole (11a) to connect the semiconductor chip (13)'s electrode (not shown in drawing) with the corresponding wire conductor (12), and (15) is a chip coat consisting of a resin such as silicone, epoxy, etc. and covering from inside the through hole (11a) to specified parts of the surrounding semiconductor chip (13)'s electrode formation region, bonding wire (14), and wire conductor (12) and protecting the semiconductor chip (13) from external air.

With the embodiment thus constituted, the semiconductor chip (13) electrodes and the wire conductors (12) corresponding to them are connected by bonding wires (14) passing inside the through hole (11a), whose shape is smaller than the external dimensions of the semiconductor chip (13), so the mounting area of the semiconductor chip (13) on the circuit board (11) can be nearly the same as the mounting area when using the flip chip system while still using the wire bonding system, and miniaturization of the circuit board (11) can be achieved. Also, the price of the semiconductor chip (13) can be cheaper than the price of a projecting-electrode type of semiconductor chip (13) used in the flip chip system, and moreover the manufacturing yield is better than the manufacturing yield when using the flip chip system, so cost reduction can be achieved. In addition, the bonding area between the chip coat (15) and the circuit board (11) can be made smaller than in the conventional example shown in FIG. 1, so stress created within the chip coat (15) by the difference in their coefficients of thermal expansion is smaller than that in the conventional example shown in FIG. 1, and the risk of breaking the bonding wire (14) due to this stress is reduced, and reliability increases.

FIG. 4 [sic] is a sectional view showing the mounting part of a semiconductor chip on a circuit board in an HIC that is another embodiment of the present invention.

In the drawing, codes that are the same as the codes in the embodiment shown in FIG. 2 indicate equivalent parts, and explanation thereof shall be omitted. (16) is an insulator whose thickness is greater than the thickness of the semiconductor chip (13) and which has a through hole (16a) whose shape is larger than the outer dimensions of the semiconductor chip (13) formed therein; it is secured to the circuit board (11) and the semiconductor chip (13), which is bonded to the circuit board (11), is inserted into the through hole (16a). This insulator (16) has the function of keeping the semiconductor chip (13) from being struck by external bodies and damaged.

An embodiment with this sort of constitution has the same effect as the embodiment shown in FIG. 2, and the semiconductor chip (13) is protected by the insulator (16), so handling it during shipping and so forth is easy.

In this embodiment the insulator (16) is secured to the circuit board (11), but the insulator (16) may also be structurally integrated with the circuit board (11).

Furthermore, the chip coat (15) was provided in each of the aforesaid embodiments, but it is not always necessary to provide the chip coat (15). If the semiconductor chip (13) is protected from external air by a glass film or the like, the chip coat (15) may be dispensed with. Also, the peripheral part of the semiconductor chip (13) was secured to the circuit board (11) using adhesive in each of the aforesaid embodiments, but this is not always limited to adhesive. The peripheral part of the semiconductor chip (13) may be secured to the circuit board (11) using a solder material such as solder, or some of the plurality of electrodes of the semiconductor chip (13) can be disposed at the peripheral part of the semiconductor chip (13), with these electrodes disposed at the peripheral part made into projecting electrodes, and the peripheral part of the semiconductor chip (13) can be secured to the circuit board (11) using these projecting electrodes.

As explained above, in the inventive HIC a through hole having a specified shape is formed in a circuit board on whose first surface wire conductors are formed, electrodes are formed within a region in the center of a semiconductor chip's main surface having the same shape as the shape of the aforesaid through hole, the peripheral part of the aforesaid semiconductor chip's main surface is secured to the aforesaid circuit board's second surface so that the aforesaid through hole and the aforesaid electrode formation region coincide, and the aforesaid electrodes of the aforesaid semiconductor chip and the aforesaid wire conductors are connected by bonding wires passing inside the aforesaid through hole, so the mounting area of the aforesaid semiconductor chip on the aforesaid circuit board can be approximately nearly the same as the mounting area when using the flip chip system while still using the wire bonding system, and the aforesaid circuit board can be miniaturized. Also, the price of the aforesaid semiconductor chip can be made cheaper than the price of a projecting-electrode type of semiconductor chip used in the flip chip system, and moreover the manufacturing yield is better than the manufacturing yield with the flip chip system, so the price can be reduced.

4. BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(A) is a plan view showing the mounting part of a semiconductor chip on a circuit board in one example of a conventional HIC. FIG. 1(B) is a sectional view along line IB-IB in FIG. 1(A). FIG. 2(A) is a plan view showing the mounting part of a semiconductor chip on a circuit board in an HIC that is one embodiment of the present invention. FIG. 2(B) is a sectional view along line IIB-IIB in FIG. 2(A). FIG. 3 is a sectional view showing the mounting part of a semiconductor chip on a circuit board in an HIC that is another embodiment of the present invention.

In the drawings, (11) is a circuit board, (11a) is a through hole, (12) is a wire conductor, (13) is a semiconductor chip, (14) is a bonding wire, (16) is an insulator, and (16a) is a through hole.

Furthermore, codes that are the same within drawings indicate identical or equivalent parts.

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FIG. 1

FIG. 2

FIG. 3

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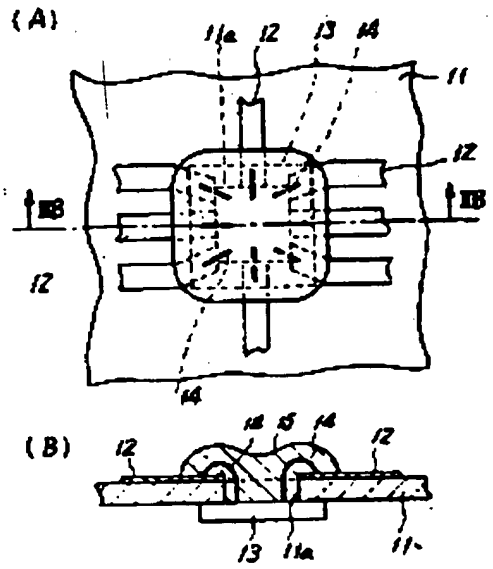
(54) HYBRID INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To reduce the area to be occupied by a circuit board by a method wherein a hole smaller in size than the semiconductor chip to be attached to the periphery of the hole is provided on the circuit board, a multiplicity of wiring conductors are fixed to the periphery of the hole, the semiconductor chip is bonded to the rear-side opening of the through hole, and the electrodes of the chip are connected to the front-side wiring conductors by means of wires running through the hole.

CONSTITUTION: A hole 11a with its size smaller than a semiconductor chip 13 is cut through a circuit board 11, and wiring conductors 12 extend outward on the circuit board 11 from the periphery of the hole 11a. The periphery of the chip 13 is fixed with an adhesive tightly to the periphery of the rear-side opening of the through hole 11a and wires 14 are connected to the electrodes provided on the chip 13. The wires 14 are let through the hole 11a to be bonded to the wiring conductors 12 on the front side of the circuit board 11. A process follows wherein the upper surface of the chip 13, and the wires 14 are sealed by the sealant 15 such as silicone or epoxy. A wire-bonded device designed in this way occupies only the same package area as a flip-chip does regardless of its nature.



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⑤4混成集積回路装置

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明 細 書

1. 発明の名称

混成集積回路装置

2. 特許請求の範囲

(1) 所要部分に所定形状を有する貫通孔が形成された回路基板、この回路基板の第1の表面上に上記貫通孔の周縁から伸びるように設けられた配線導体、一方の主面の中央部の、上記貫通孔の形状と同一形状の領域内に形成された電極を有しこの電極が形成された上記領域と上記貫通孔とが一致するようにして上記主面の周縁部が上記回路基板の第2の表面に固着された半導体チップ、およびこの半導体チップの上記電極と上記配線導体とを上記貫通孔内を通して接続したボンデイングワイヤを備えた混成集積回路装置。

(2) 回路基板の第2の表面に、半導体チップの厚さより厚い厚さを有し上記第2の表面の上記半導体チップを固着すべき部位に対応する部分に上記半導体チップの外形寸法より大きい形状の貫通孔を形成した絶縁体が設けられたことを特徴とする特許請求の範囲第1項記載の混成集積回路装置。

3. 発明の詳細な説明

この発明は回路基板に半導体チップおよび外付け部品を装着してなる混成集積回路装置(以下「HIC」と呼ぶ)に関するものである。

第1図(A)は従来のHICの一例の半導体チップの回路基板への装着部を示す平面図、第1図(B)は第1図(A)のIB—IB線での断面図である。

図において、(1)は表面の一部に凹部(1a)が設けられた回路基板、(2)は回路基板(1)の表面上に凹部(1a)の側壁の上端から伸びるように形成された複数個の配線導体、(3)は第1の主面の端縁に沿い互いに所定間隔をおいて複数個の電極(図示せず)が形成され第2の主面が凹部(1a)の底面に固着された半導体チップ、(4)は半導体チップ(3)の電極(図示せず)とこれに対応する配線導体(2)とを接続するボンデイングワイヤ、(5)はシリコーン,エポキシなどの樹脂からなり凹部(1a)内からその周辺の回路基板(1)の表面上の一部にわたつて、半導体チップ(3),ボンデイングワイヤ(4)および配線導体

(2)の所要部分を覆うように施され外気から半導体チップ(3)を保護するチップコートである。

ところで、この従来例のHICでは、半導体チップ(3)の第2の主面を回路基板(1)の凹部(1a)の底面にろう接して半導体チップ(3)の各電極とこれらの電極にそれぞれ対応する配線導体(2)とをボンディングワイヤ(4)で接続するいわゆるワイヤボンディング方式であるので、半導体チップ(3)の回路基板(1)への実装面積が半導体チップ(3)の主面の面積より大きくなる。従つて、時計などに用いるHICのように、回路基板(1)の小形化が要求される場合には不利であるという問題があつた。その上、チップコート(5)の回路基板(1)との接着面積も大きくなるので、回路基板(1)の熱膨張係数とチップコート(5)の熱膨張係数との差によつてチップコート(5)内に大きな応力が生じ、この応力によつてボンディングワイヤ(4)が断線するおそれがあり、信頼性が悪いという問題もあつた。このような問題を解決するために、従来、半導体チップ(3)の複数個の電極をすべて突起電極にして、これらの突起電極をそれぞれの対応する配線導体(2)に同時にろう接するいわゆるフリップチップ方式が用いられている。ところが、このフリップチップ方式では、突起電極にした半導体チップ(3)の回路基板(1)への実装面積が半導体チップ(3)の主面の面積と同一になるので、回路基板(1)を小形化することができるが、突起電極にした半導体チップ(3)の価格がワイヤボンディング方式に用いる突起電極にしない半導体チップ(3)の価格より著しく高くなる。その上、突起電極にした半導体チップ(3)の各突起電極をそれぞれの対応する配線導体(2)に同時に満足すべき状態でろう接することは容易ではないので、フリップチップ方式での製造歩留りがワイヤボンディング方式での製造歩留りより悪く、製造コストも高くなるという欠点があつた。

この発明は、上述の欠点に鑑みてなされたもので、ワイヤボンディング方式を用いながら半導体チップの回路基板への実装面積を小さくできるように半導体チップおよび回路基板の構造を改良することによつて、回路基板の形状を小形化するとともに価格を安くしたHICを提供することを目的とする。

第2図(A)はこの発明の一実施例のHICの半導体チップの回路基板への装着部を示す平面図、第2図(B)は第2図(A)のⅡB－ⅡB線での断面図である。

図において、(11)は所要部分に所定形状を有する貫通孔(11a)が形成された回路基板、(12)は回路基板(11)の第1の表面上に貫通孔(11a)の周縁から伸びるように形成された複数個の配線導体、(13)は一方の主面の中央部の、貫通孔(11a)の形状と同一形状の領域内に複数個の電極(図示せず)が形成された半導体チップで、この半導体チップ(13)の電極形成領域が貫通孔(11a)と一致するようにして半導体チップ(13)の周縁部が回路基板(11)の第2の表面に接着剤で接着されている。(14)は半導体チップ(13)の電極(図示せず)とこれに対応する配線導体(12)とを貫通孔(11a)内を通して接続するボンディングワイヤ、(15)はシリコーン、エポキシなどの樹脂からなり貫通孔(11a)内からその周辺の回路基板(11)の第1の表面上の一部にわたつて、半導体チップ(13)の電極形成領域、ボンディングワイヤ(14)および配線導体(12)の所要部分を覆うように施され外気から半導体チップ(13)を保護するチップコートである。

このように構成されたこの実施例では、半導体チップ(13)の外形寸法より小さい形状の貫通孔(11a)内を通して半導体チップ(13)の電極とこれに対応する配線導体(12)とをボンディングワイヤ(14)で接続するので、ワイヤボンディング方式でありながら半導体チップ(13)の回路基板(11)への実装面積を、フリップチップ方式の場合の実装面積とほぼ同一にすることができ、回路基板(11)の小形化を図ることができる。また、半導体チップ(13)の価格を、フリップチップ方式に用いる突起電極にした半導体チップ(13)の価格より安くすることができ、しかも製造歩留りをフリップチップ方式の場合の製造歩留りよりよくすることができるので、価格の低減を図ることができる。更に、チップコート(15)の回路基板(11)との接着面積を、第1図に示した従来例のそれより小さくすることができるので、これらの間

の熱膨張係数の差によつてチップコート06内に生ずる応力が第1図に示した従来例のそれより小さくなつて、この応力によつてボンディングワイヤ04が断線するおそれが少なくなり、信頼性を向上させることができる。

第4図はこの発明の他の実施例のHICの半導体チップの回路基板への装着部を示す断面図である。

図において、第2図に示した実施例の符号と同一符号は同等部分を示し、その説明は省略する。06は半導体チップ03の厚さより厚い厚さを有し半導体チップ03の外形寸法より大きい形状の貫通孔(16a)が形成され貫通孔(16a)内に回路基板01に装着された半導体チップ03を挿入させて回路基板01に固着された絶縁体で、この絶縁体06は半導体チップ03が外部物体と衝突して損傷するのを防止する役目をする。

このようなこの実施例の構成では、第2図に示した実施例と同様の効果がある上に、絶縁体06によつて半導体チップ03が保護されているので、搬送時における取り扱いなどが容易になる。

この実施例では、絶縁体06を回路基板01に固着したが、絶縁体06を回路基板01と一体構造にしてもよい。

なお、上記各実施例では、チップコート06を設けたが、必ずしもチップコート06を設ける必要はなく、半導体チップ03がガラス被膜などによつて外気から保護されている場合にはチップコート06を省略してもよい。また、上記各実施例では、半導体チップ03の周縁部を接着剤を用いて回路基板01に固着したが、必ずしもこれは接着剤に限定する必要はなく、半導体チップ03の周縁部を半田などのろう材を用いて回路基板01に固着するようにしてもよく、もしくは半導体チップ03の複数個の電極のうちの一部を半導体チップ03の周縁部に配設し、この周縁部に配設された電極を突起電極にして、この突起電極を用いて半導体チップの周縁部を回路基板01に固着するようにしてもよい。

以上、説明したように、この発明のHICでは、第1の表面上に配線導体が形成された回路基板に所定形状の貫通孔を形成し、半導体チップの主面の中央部の上記貫通孔の形状と同一形状の領域内に電極を形成し、上記貫通孔と上記電極形成領域とが一致するようにして上記半導体チップの上記主面の周縁部を上記回路基板の第2の表面に固着して、上記半導体チップの上記電極と上記配線導体とを上記貫通孔内を通してボンディングワイヤで接続するので、ワイヤボンディング方式でありながら上記半導体チップの上記回路基板への実装面積をフリップチップ方式の場合の実装面積とほぼ同一程度にすることができ、上記回路基板の小形化を図ることができる。また、上記半導体チップの価格をフリップチップ方式に用いる突起電極にした半導体チップの価格より安くすることができ、しかも製造歩留りをフリップチップ方式の場合の製造歩留りよりよくすることができるので、価格の低減を図ることができる。

4. 図面の簡単な説明

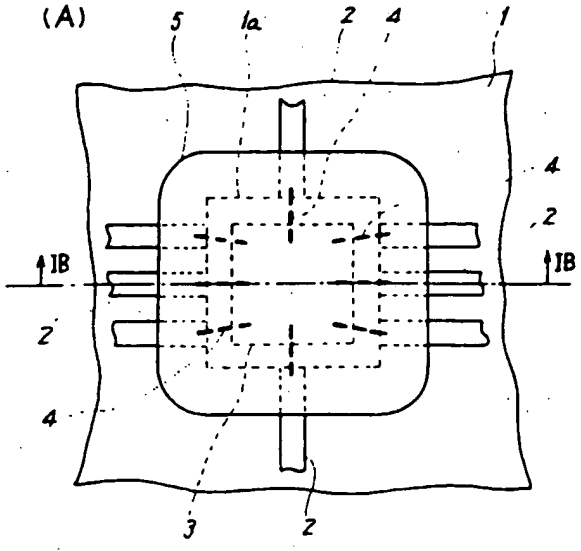
第1図(A)は従来のHICの一例の半導体チップの回路基板への装着部を示す平面図、第1図(B)は第1図(A)のIB−IB線での断面図、第2図(A)はこの発明の一実施例のHICの半導体チップの回路基板への装着部を示す平面図、第2図(B)は第2図(A)のIIB−IIB線での断面図、第3図はこの発明の他の実施例のHICの半導体チップの回路基板への装着部を示す断面図である。

図において、01は回路基板、(11a)は貫通孔、02は配線導体、03は半導体チップ、04はボンディングワイヤ、06は絶縁体、(16a)は貫通孔である。

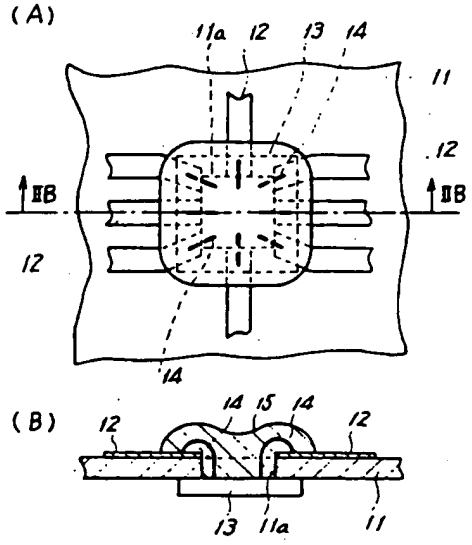
なお、図中同一符号はそれぞれ同一もしくは相当部分を示す。

代理人　葛野信一(外1名)

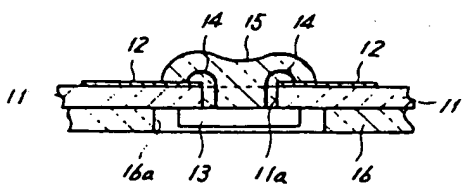
第 1 図


(A)
5
1a
2
4
1
4
2
IB
IB
2
4
3
2
(B)
2
4
5
4
2
1
3
1a

第 2 図


(A)
11a
12
13
14
11
12
IIB
IIB
12
14
(B)
14
15
14
12
12
13
11a
11

第 3 図


14
15
14
12
12
11
11
16a
13
11a
16